FORM PTO-1390 (REV 10-2000) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY'S DOCKET NUMBER: Klemt 1

U.S. APPLICATION NO. (If known, see 37 CFR 1.5): Unknown 09/913364

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/DE00/00368	7 February 2000	10 February 1999

TITLE OF INVENTION: A SWITCHING ARRANGEMENT FOR GALVANICALLY INSULATED CONTROL OF A LOAD-CONTROLLED POWER SWITCH

APPLICANT(S) FOR DO/EO/US: Michael Klemt, et al

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☒ This is an express request to promptly begin national examination procedures (35 U.S.C. 371(f)).
4. ☒ The US has been elected by the expiration of 19 months from the priority date (PCT Article 31).
5. ☒ A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   a. ☐ is attached hereto (required only if not communicated by the International Bureau).
   b. ☒ has been communicated by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☒ An English language translation of the International Application as filed (35 U.S.C. 371(c)(2)).
7. ☐ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))
   a. ☐ are attached hereto (required only if not communicated by the International Bureau).
   b. ☐ have been communicated by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☐ have not been made and will not be made.
8. ☐ An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. ☒ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
10. ☐ An English language translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11 to 16 below concern document(s) or information included:

11. ☐ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
12. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. ☒ A FIRST preliminary amendment.
    ☐ A SECOND or SUBSEQUENT preliminary amendment.
14. ☐ A substitute specification.
15. ☐ A change of power of attorney and/or address letter.
16. ☐ Other items or information:

"Express Mail" Mailing Label Number EL 490 189 201 US

Date of Deposit August 10, 2001

I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to the Commissioner of patents and trade marks, Washington, D.C. 20231.

Mary Ann Copas

Mary Ann Copas, Sec'y

U.S. APPLICATION NO. (If known, see 37 CFR 1.5)	INTERNATIONAL APPLICATION NO.	ATTORNEY'S DOCKET NUMBER
Unknown 09/914336	PCT/DE00/00368	Klemt 1

17. ☒ The following fees are submitted:	CALCULATIONS PTO USE ONLY	
BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)) :		
Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO **$1000.00**		
International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO **$860.00**		
International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO **$710.00**		
International preliminary examination fee paid to USPTO (37 CFR 1.482) but all claims did not satisfy provisions of PCT Article 33(1)-(4) **$690.00**		
International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(1)-(4) **$100.00**		
ENTER APPROPRIATE BASIC FEE AMOUNT =	$ 860.00	
Surcharge of **$130.00** for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(e)).	$	

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE		
Total claims	16 - 20 =		X **$18.00**	$	
Independent claims	4 - 3 =	1	X **$80.00**	$ 80.00	
MULTIPLE DEPENDENT CLAIM(S) (if applicable)			+ **$270.00**	$	
TOTAL OF ABOVE CALCULATIONS =				$ 940.00	
☒ Applicant claims small entity status. See 37 CFR 1.27. The fees indicated above are reduced by 1/2.				$ 470.00	
SUBTOTAL =				$ 470.00	
Processing fee of **$130.00** for furnishing the English translation later than ☐20 ☐30 months from the earliest claimed priority date (37 CFR 1.492(f)). +				$	
TOTAL NATIONAL FEE =				$ 470.00	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). **$40.00** per property +				$	
TOTAL FEES ENCLOSED =				$ 470.00	
				Amount to be refunded:	$
				charged:	$

a. ☒ A check in the amount of $ 470.00 to cover the above fees is enclosed.

b. ☐ Please charge my Deposit Account No. _____ in the amount of $_____ to cover the above fees. A duplicate copy of this sheet is enclosed.

c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 02-1653. A duplicate copy of this sheet is enclosed. In the event there is any discrepency in the amount sent herewith or at any time in the future please charge any additional fee, credit or overpayment to the above deposit account number.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

ROBERT W. BECKER & ASSOCIATES
11896 N. HIGHWAY 14 SUITE B
TIJERAS, NEW MEXICO 87059

Robert W. Becker
SIGNATURE:

Robert W. Becker
NAME

26,255
REGISTRATION NUMBER

CONTINUED PROSECUTION APPLICATION (CPA) REQUEST TRANSMITTAL

"Express Mail" Mailing Label Number EL 490 189 201 US
Date of Deposit August 10, 2001
I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to the Commissioner of Patents and Trademarks, Washington, D.C. 20231.

Mary Ann Copas, Secretary

Address to:	Attorney Docket No.	DIE14483-USCPA
Assistant Commissioner of Patents BOX CPA Washington, DC 20231	First Named Inventor:	Rudolf Supe-Dienes
	Examiner:	Clark Dexter
	Group/Art Unit:	3724

This is a Request for a [X] continuation or [ ] divisional application under 37 CFR 1.53(d), (continued prosecution application (CPA)) of prior U.S. Application No. 09/251,781, filed February 17, 1999, entitled:

BLADE HOLDER WITH CUTTING FORCE ADJUSTMENT INDEPENDENT OF STROKE

1. [X] Enter the unentered amendment previously filed on July 10, 2001 under 37 CFR 1.116 in the prior nonprovisional application.

2. [ ] A preliminary amendment is enclosed.

3. [ ] This application is being filed by fewer than all the inventors named in the prior application, 37 CFR 1.53(d)(4).
   a. [ ] ***DELETE*** the following inventor(s) named in the prior nonprovisional application:
   b. [ ] The inventor(s) to be deleted are set forth on a separate sheet attached hereto.

4. [ ] A new power of attorney or authorization of agent (PTO/SB/81) is enclosed.

5. [ ] Information Disclosure Statement (IDS) is enclosed:
   a. [ ] PTO-1449
   b. [ ] Copies of IDS Citations

CLAIMS	(1) FOR	(2) NUMBER FILED	(3) NUMBER EXTRA	(4) RATE	(5) CALCULATIONS
	TOTAL CLAIMS	4 - 20 =	0	x $18 =	0
	INDEPENDENT CLAIMS	1 - 3 =	1	x $80 =	0
	MULTIPLE DEPENDENT CLAIM(S) (if applicable)			$ =	0
			BASIC FEE		$710.00
			Total of above Calculations =		$710.00
	Reduction by 1/2 for filing by small entity (Note 37 CFR 1.9, 1.27, 1.28).				$355.00
				TOTAL	$355.00

6. [x] Small Entity status:

a. [ ] A small entity statement is enclosed.
b. [x] A small entity statement was filed in the prior nonprovisional application and such status is still proper and desired.
c. [ ] Is no longer claimed.

7. [X] It is respectfully requested that, if necessary to effect a timely response in application Serial No. 09/251,781 filed on February 17, 1999, and/or the instant continued prosecution application, this paper be considered as a **Petition for an Extension of Time** sufficient to effect a timely response **at any time during prosecution**. The Commissioner is hereby authorized to credit overpayments or charge the following fees, if not submitted by check, or shortages in any fees to **Deposit Account 02-1653**:

Fees required under 37 CFR 1.16;
Fees required under 37 CFR 1.17;
Fees required under 37 CFR 1.18.

8. [X] A check in the amount of $410.00 is enclosed (basic filing fee $355.00 and one-month time extension fee $55.00).

9. [X] The power of attorney in the prior application is to:
Robert W. Becker, Reg. No. 26,255 of ROBERT W. BECKER & ASSOCIATES, 11896 N. Highway 14, Suite B, Tijeras, NM 87059.

10.[X] Other:

Petition and fee for one month time extension ($55.00).

Please address all future communications to: (May only be completed by applicant, or attorney or agent of record.)

ROBERT W. BECKER & ASSOCIATES, 11896 N. Highway 14, Suite B, Tijeras, New Mexico 87059 Telephone (505) 286-3511 (Facsimile: (505) 286-3524).

August 10, 2001
Date

Robert - Becker
Signature of Attorney or Agent of Record

Robert W. Becker
Typed or Printed name

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In the Application of Michael Klemt, et al

Ser. No.: Not Yet Known (based on DE 199 05 500.0 filed 10 February 1999, DE199 63 330.4 filed 27 December 1999 and PCT/DE00/00368 filed 7 February 2000)

International Filing Date: 7 February 2000

For: A SWITCHING ARRANGEMENT FOR GALVANICALLY INSULATED CONTROL OF A LOAD-CONTROLLED POWER SWITCH

Box PCT
Assistant Commissioner for Patents
Washington, DC 20231

PRELIMINARY AMENDMENT ACCOMPANYING ENTRY INTO NATIONAL STAGE APPLICATION

Sir:

Prior to examination, please amend the above-identified application as follows.

IN THE SPECIFICATION:

On page 1, immediately after the title, please insert the following heading:

--Background of the Invention--.

On page 2, between lines 11 and 12, please insert the following heading:

--Summary of the Invention--;

Page 2, between lines 16 and 17, please delete "This object is realized by the characterizing features of patent claims one to seven. Advantageous embodiments of the invention are contained in the dependent claims."

On page 3, between lines 15 and 16, please insert the following heading:

--Brief Description of the Drawings--.

Page 5, between lines 20 and 21, please insert the following heading:

--Description of Preferred Embodiments--.

On page 13, at the bottom of the page please insert the following paragraph:

--The specification incorporates by reference the disclosure of German priority documents199 05 500.9 of 10 February 1999, 199 63 330.4 of 27 December 1999 and PCT/DE00/00368 of 7 February 2000.

The present invention is, of course, in no way restricted to the specific disclosure of the specification and drawings, but also encompasses any modifications within the scope of the appended claims.--

IN THE CLAIMS:

Please cancel claims 1 - 16, and replace them with the attached claims 17 - 32.

REMARKS

Claims 17 - 32 are pending in the application.

Appropriate headings have been added to the specification, and the abstract and claims from the literal translation have been replaced by an abstract and claims drafted in conformity with U.S. Patent practice.

The application in its amended state is believed to be in condition for allowance. However, should the Examiner have any comments or suggestions, or wish to discuss the merits of the application, the undersigned would very much welcome a telephone call in order to expedite placement of the application into condition for allowance.

Respectfully submitted,

Robert W. Becker Reg. No. 26,255
for Applicant(s)

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RWB:els

WHAT WE CLAIM IS:

17. A switching arrangement for controlling load-controlled power switches via a transformer which generates positive and negative voltage impulses, comprising:

a transformer for generating positive and negative impulses, the transformer having a primary and a secondary side, the secondary side having discharge circuits and an input for inputting therein voltage impulses in positive and negative directions and having short durations,

two field effect transistors each having a source terminal and a drain terminal, the field effect transistors being connected to the discharge circuits at the secondary side of the transformer and being operable to convert the inputted voltage impulses into voltage impulses in positive and negative directions for controlling the power switch, the impulse duration of the voltage impulses being extended to the beginning of the next input impulses with reversed voltage directions, the source terminal of the first field effect transistor being connected with a discharge circuit and the source terminal of the second field effect transistor being connected with a different discharge circuit, the drain terminal of the first field effect transistor being connected with the gate terminal of the power switch and the drain terminal of the second field effect transistor being connected with a further terminal of the power switch and the gate terminal of the first field effect transistor

being connected via a first resistor with the drain terminal of the second field effect transistor and the gate terminal of the second field effect transistor being connected via a second resistor with the drain terminal of the first field effect transistor.

18. A switching arrangement according to 17, a respective zener diode is connected in series with each of the first and second resistors.

19. A switching arrangement for controlling load-controlled power switches via a transformer which generates positive and negative voltage impulses, comprising:

a transformer for generating positive and negative impulses, the transformer having a primary and a secondary side, the secondary side having discharge circuits and an input for inputting therein voltage impulses in positive and negative directions and having short durations,

two field effect transistors each having a source terminal and a drain terminal, the field effect transistors being connected to the discharge circuits at the secondary side of the transformer and being operable to convert the inputted voltage impulses into voltage impulses in positive and negative directions for controlling the power switch, the impulse duration of the voltage impulses being extended to the beginning of the next input impulses with reversed voltage directions, the source terminal of the first field effect transistor being connected

with a discharge circuit and the source terminal of the second field effect transistor being connected with a different discharge circuit, the drain terminal of the first field effect transistor being connected with the gate terminal of the power switch and the drain terminal of the second field effect transistor being connected with a further terminal of the power switch, the gate terminal of the first field effect transistor being connected via a series switch having a first resistor and a first zener diode with the source terminal of the second field effect transistor and the gate terminal of the second field effect transistor being connected via a series switch having a second resistor and a second zener diode with the source terminal of the first field effect transistor.

20. A switching arrangement for controlling load-controlled power switches via a transformer which generates positive and negative voltage impulses, comprising:

a transformer for generating positive and negative impulses, the transformer having a primary and a secondary side, the secondary side having discharge circuits and an input for inputting therein voltage impulses in positive and negative directions and having short durations,

two field effect transistors each having a source terminal and a drain terminal, the field effect transistors being connected to the discharge circuits at the secondary side of the transformer and being operable to convert the inputted voltage impulses into voltage impulses

in positive and negative directions for controlling the power switch, the impulse duration of the voltage impulses being extended to the beginning of the next input impulses with reversed voltage directions, the source terminal of the first field effect transistor being connected with a discharge circuit and the source terminal of the second field effect transistor being connected with a different discharge circuit, the drain terminal of the first field effect transistor being connected with the gate terminal of the power switch and the drain terminal of the second field effect transistor being connected with a further terminal of the power switch and the gate terminal of the first field effect transistor being connected via a series switch having a first resistor and a first zener diode with the source terminal of the second field effect transistor and the gate terminal of the second field effect transistor being connected via a second resistor with the drain terminal of the first field effect transistor.

21. A switching arrangement according to claim 20, wherein a second zener diode is connected in series with the second resistor.

22. A switching arrangement for controlling load-controlled power switches via a transformer which generates positive and negative voltage impulses, comprising:

a transformer for generating positive and negative impulses, the transformer having a primary and a secondary side, the secondary side having discharge circuits and an input for inputting

therein voltage impulses in positive and negative directions and having short durations,

two field effect transistors each having a source terminal and a drain terminal, the field effect transistors being connected to the discharge circuits at the secondary side of the transformer and being operable to convert the inputted voltage impulses into voltage impulses in positive and negative directions for controlling the power switch, the impulse duration of the voltage impulses being extended to the beginning of the next input impulses with reversed voltage directions, the source terminal of the first field effect transistor being connected with a discharge circuit and the source terminal of the second field effect transistor being connected with a different discharge circuit, the drain terminal of the first field effect transistor being connected with the gate terminal of the power switch and the drain terminal of the second field effect transistor being connected with a further terminal of the power switch and the gate terminal of the first field effect transistor being connected via a first resistor with the drain terminal of the second field effect transistor and the gate terminal of the second field effect transistor being connected via a series switch having a second resistor and a second zener diode with the source terminal of the first field effect transistor.

23. A switching arrangement according to claim 22, wherein a first zener diode is connected in series with the first resistor.

24. A switching arrangement according to claim 16, wherein a third resistor is connected between the gate terminal and a further terminal of the power switch.

25. A switching arrangement according to claim 16, wherein a MOS-FET (metal oxide semiconductor field effect transistor) or an IGBT (insulated gate bipolar transistor) is used as the power switch.

26. A switching arrangement according to claim 16, wherein the duration of the voltage impulse inputted into the input of the transformer does not exceed five µs and is less than or equal to the duration of the activation impulse and less than or equal to the de-activation impulse of the power switch.

27. A switching arrangement according to claim 16, wherein a respective diode is disposed between each of the field effect transistors between the source terminal and the drain terminal thereof.

28. A switching arrangement according to claim 16, wherein an input capacitor is disposed in the power switch between the gate terminal and a further terminal.

29. A switching arrangement according to claim 16, wherein the two field effect transistors effect a transformation of the two input impulses into respective longer impulses of which one effects the activation of power switch and the maintenance of the power switch in its activated condition and the other effects the de-activation of the

power switch and maintenance of the power switch in its de-activated condition.

30. A switching arrangement according to 29, wherein the duration of the period of the impulse inputted into the input of the transformer corresponds to the durations of the periods of the impulses which effect the control of the power switch.

31. A switching arrangement according to claim 16, wherein the durations of the periods of the impulse at the power switch can have a predetermined relationship with one another (duty cycle).

32. A switching arrangement according to claim 16, wherein the use of a transformer with oppositely sensed windings of the primary and secondary sides thereof determines the voltage direction of the impulse at the power switch.

A SWITCHING ARRANGEMENT FOR GALVANICALLY INSULATED CONTROL OF A LOAD-CONTROLLED POWER SWITCH

The present invention relates to a switching arrangement for controlling a load-controlled power switch via a transformer with positive and negative voltage impulses.

In a switching arrangement of this type, the impulse is transferred from the primary side of the transformer to the secondary side thereof. This transfer can only be accomplished in an error free manner if the voltage time surfaces of the positive and negative voltage impulses are the same. A power switch requires, for its activation, a positive voltage impulse and, for its de-activation, a negative voltage impulse. In most cases, during periods of the same duration, the relationship between the length or duration of the positive and negative impulses (the duty cycle) changes so that the voltage time surfaces are not equal and the transformer, following a certain time, is saturated. This leads to the consequence that the voltage at the input of the transformer breaks through, or the amplitudes change, in the event that a capacitor is connected in series to an input on the primary side of the transformer. It has also not been heretofore possible to generate, with the help of a transformer, the voltages required for the activation and de-activation of a power switch such

that these voltage impulses are generated in a consistently error-free manner and have the desired duty cycle.

JP 62-25418A discloses a gate driver circuit in which two field effect transistors are disposed on the secondary side of the transformer, the gate terminals of the field effect transistors being coupled directly to the discharge circuits of the transformer.

WO 9311609A1 discloses a switching arrangement in which two different impulse series having differing amplitudes are inputted into the input of the transformer, whereby only the positive impulses of the first impulse series and only the negative impulses of the second impulse series are rectified on the secondary side of the transformer.

The present invention offers a solution to the challenge of providing, in a transformer, short time impulses which do not lead to saturation of the transformer, and providing a preparation of the inputted impulses to the secondary side of the transformer such that the power switch is reliably activated and de-activated.

This object is realized by the characterizing features of patent claims one to seven. Advantageous embodiments of the invention are contained in the dependent claims.

The important advantage of the invention is comprised in the fact that the inputting of only short time input impulses to the activated field effect transistors on the secondary side of the transformer

produces the required longer impulses which ensure the reliable activation and de-activation of the power transistors. Only short impulses are therefore inputted into the transformer, which cannot lead to a saturation of the transformer. If an impulse in the positive direction is at the secondary side of the transformer, one of the two field effect transistors is activated and the free running diode of the other transistor is driven in a forward or pass direction so that the voltage at the secondary side of the transformer is disposed at the power transistor which is to be activated. In connection with an impulse in the negative direction, the transistors perform an opposite function so that the negative voltage is disposed at the power transistor to be activated. If no impulse is provided, the free running diode no longer runs in the forward or pass direction but, instead, is driven in the blocking direction, whereby the voltage at the gate of the power switch remains available as the charge carrier cannot drain.

The present invention is described in further detail in connection with switching configurations shown in the figures of the drawings. The figures of the drawings are:

Fig. 1 shows a power switch connected with a transformer in accordance with the prior art.

Fig. 2 shows the switching arrangement of the present invention for controlling a power switch, whereby

the gate terminals of the field effect transistors disposed on the secondary side of the transformer are connected via a series circuit comprising a resistor and a zener diode with the drain terminals of the respective other field effect transistors.

Fig. 3 shows a further embodiment of the switching arrangement of the present invention for controlling a power switch, whereby the gate terminals of the two field effect transistors on the secondary side of the transformer are connected via a series circuit comprising a resistor and a zener diode with the source terminals of the respective other field effect transistor.

Fig. 4 shows a further embodiment of the switching arrangement of the present invention for controlling a power switch, whereby the gate terminal of the first field effect transistor is connected via a series switch comprising a resistor and a zener diode with the source terminal of the second field effect transistor and the gate terminal of the second field effect transistor is connected via a series switch comprising a resistor and a

zener diode with the drain terminal of the first field effect transistor.

Fig. 5 shows a further embodiment of the switching arrangement of the present invention for controlling a power switch, whereby the gate terminal of the first field effect transistor is connected via a series switch comprising a resistor and a zener diode with the drain terminal of the second field effect transistor and the gate terminal of the second field effect transistor is connected via a series switch comprising a resistor and a zener diode with the source terminal of the first field effect transistor.

Fig. 6 shows in a diagram the arrangement of the voltage impulses inputted into the transformer as a function of time and

Fig. 7 shows in a diagram as a function of time the voltage impulse which, following their preparation by the field effect transistors in the secondary region of the transformer, are at the power switch.

As seen in Fig. 1, in a conventional switching arrangement, a signal Ua is transferred via a transformer Ü to a power switch LT. If

the signal on the primary side of the transformer Ü is to be transferred in an error-free manner to the secondary side of the transformer, the voltage time surfaces of the positive and negative voltage impulses must be the same magnitude. In the event of unequal magnitudes of the voltage time surfaces, the transformer, after the passage of a certain time, will be saturated, which leads to the consequence that the voltage impulses no longer possess the desired plot or form.

As seen in Fig. 2, in one embodiment of the switching arrangement of the present invention, the field effect transistors F1 and F2 are activated in the discharge outlets Ü1 and Ü2 of the secondary portion of the transformer Ü. The field effect transistor F1 is disposed with its source terminal S and its drain terminal D connected via an intermediary circuit to an internal diode D1 directly in the discharge circuit Ü1. The gate terminal G of the field effect transistor F1 is connected via an intermediary circuit of a resistor R1 and a zener diode Z1 to the drain terminal D of the field effect transistor F2. The field effect transistor F2 is disposed in the same directional sense with its source terminal S and its drain terminal D via an intermediary circuit of an internal diode D2 in the discharge circuit Ü2. The gate terminal G of the second field effect transistor F2 is connected via an intermediary circuit comprising a resistor R2 and a zener diode Z2 to the drain terminal D of the field effect transistor F1. The gate terminal

G of the power switch LT is connected with the drain terminal D of the field effect transistor F1, and the source terminal S of the power switch is connected to the drain terminal D of the second field effect transistor F2. An input capacitor C and a resistor R3 are connected in parallel between the gate terminal G and the source terminal S of the power transistor LT.

The function of the switching arrangement shown in Fig. 2 is as follows: in the input of the transformer Ü, a voltage signal U1 comprising positive impulses (amplitude U1p, duration T1p) and negative impulses (amplitude U1 and, duration T1) are inputted (see Figure 6). In this connection, the duration of the period T of the voltage signal U1 corresponds to the length of the impulse that is prepared on the secondary side of the transformer Ü for controlling the power switch LT for the required period T (T3p, T3n, see Figure 7). The impulses T1p and T1n have the same amplitude and duration, whereby these impulses are purposely configured to have a duration precisely as long as the switching operations of the power switch which is to be controlled, which thereby offers the advantage that, during this critical phase, the power switch sees a low resistance or low impedance source – namely, the primary side impulse generator. The impulse T1p and the impulse T1n are, due to their identical short durations and the identical magnitudes of their amplitudes (i.e., the

same voltage time surfaces), transferred without distortion to the secondary side of the transformer Ü.

Upon the inputting of a positive voltage impulse U1p, the diode D1 is driven in the forward or pass direction so that a positive voltage at the gate terminal of the second field effect transistor F2 is available relative to the source terminal S of the second field effect transistor F2. In this manner, the field effect transistor F2 is activated and the drain-source extent of the second field effect transistor F2 is of low resistance or low impedance. Thereafter, a positive impulse with a voltage height U3p=U1p-UD1-UDS2 is at the power transistor LT. In this manner, the power transistor LT is activated. In this connection, the following obtains: UD1 is the voltage drop at the diode D1 in the forward or pass direction and UDS2 is the voltage drop between the drain and the source of the second field effect transistor F2. These two voltage drops are relatively small with respect to U1p, so that the voltage drop U3p is only slightly smaller than U1p. If the voltage U1p drops to zero volts (see Fig. 6), the diode D1 is driven in the blocking direction, whereby the voltage U3p at the gate terminal of the power transistor LT (the voltage at the input capacitor C) remains available at the gate terminal of the power switch LT, since the discharge via the resistor R3 only occurs over a relatively long period. In this manner, the positive voltage U3p remains in effect during the entire duration of

T3p (see Fig. 7). In this connection, it is presumed that the time constant provided by the resistor R3 and the capacitor C is more than ten times greater than that of the period T of the signal U3. Only in this manner can the discharge via the resistor R3 be omitted. The resistor R3 ensures that the gate terminal G of the power transistor LT cannot be electrostatically loaded by de-activated electronics.

In connection with the input of a negative voltage impulse U1n, the diode D2 is driven in the forward or pass direction, so that, at the gate terminal of the first field effect transistor F1, a positive voltage is available relative to the source terminal S of the first field effect transistor F1. In this manner, the field effect transistor F1 is activated and the drain-source extent of the first field effect transistor F1 is low resistance or low impedance. Thereafter, a negative impulse is disposed at the power transistor LT having a voltage height U3n=U1n+UD2+UDS1. In this manner, the power transistor LT is de-activated. In this connection, the two voltage drops UD2 and UDS1 are again relatively small with respect to U3n so that the magnitude of U3n is only slightly smaller than the magnitude of U1n. If the voltage U1n drops to zero volts (see Fig. 6), the diode D2 is driven in the blocking direction, whereby the voltage U3n (the voltage at the input capacitor C) remains at the gate of the power transistor LT, since the discharge via the resistor R3 occurs only over a relatively long period.

In this manner, the negative voltage U3n remains during the entire duration of T3n (see Fig. 7).

The resistors R1 and R2 are of a special significance: the inductance of the transformer, together with the input capacitor of the field effect transistors, which are disposed between the gate and source terminals, forms a resonant or oscillatory circuit which, without the resistors R1 and R2, would be substantially undamped. A further task of the resistors R1 and R2 is to filter the coupled, high frequency disturbance impulses in a manner such that these impulses do not reach the gate terminals of the field effect transistors F1 and F2. The zener diodes Z1 and Z2 ensure that the input threshold beyond which the field effect transistors F1 and F2 are activated, is raised to the breakdown voltage of the zener diodes. The switching arrangement is thus insensitive to disturbance impulses. These disturbance impulses occur upon the deactivation of the magnetic flow and oscillate around the null or zero point in opposite directions. Further, disturbance impulses arise through the capacitive through-coupled components of the load voltage. Without the heretofore described measures, the disturbance impulses could lead to false activation of the power switch LT.

The difference of the embodiment shown in Fig. 3 is that the gate terminals are connected via a series switch comprising a resistor

and zener diodes with the source terminals of the respective other field effect transistor. In Fig. 4, the difference in this embodiment of the switching arrangement of the present invention is that only the field effect transistor F1 is connected via a series switch comprising a resistor and a zener diode with a source terminal of the second field effect transistor F2 and, in the embodiment shown in Fig. 5, only the second field effect transistor F2 is connected via a series switch comprising a resistor and a zener diode with the source terminal of the first field effect transistor F1. If a switching arrangement is used in which one or both of the gate terminals are connected with the source terminal of the respective other field effect transistor, then, in each instance, both components (the zener diode and the resistor) in the intermediary circuit leading to the source terminal must be intermediately activated. In this event, the forward or through voltage of the free running diode (D1, D2) does not participate in the activation and/or de-activation circuit and cannot, therefore, increase the input threshold.

The switching arrangement is suitable for potential free control of load-controlled power switches, especially, MOS-field effect transistors or IGB-transistors. The signal source for the impulse on the primary side of the transformer Ü is purposely chosen to be very low resistance or very low impedance, whereby a rapid activation of the

power switch LT is made possible. If the duration of one of the impulses T3p or T3n were to be configured to be smaller than the period of the corresponding impulses T1p or T1n, respectively, then the switch component on the primary side of the transformer Ü must be configured to limit the period or duration of the impulse T1p or T1n, respectively, to that of the impulse T3p or T3n, respectively. The switching arrangement can be deployed in a multiple option manner in combination circuit components and inverters for controlling power switches.

The features recited in Claim 16 are provided by a switching arrangement having opposed winding senses on the primary and secondary sides of the transformer. The impulses on the winding outputs Ü1, Ü2 as well as the impulses T3n, T3p at the power transistor LT, have an opposite voltage direction.

By the deployment of the inventive switching arrangement for controlling a load-controlled power switch, significant advantages are realized relative to the heretofore conventional practice: plus and minus voltages are insulated in a galvanic manner during their transfer so that a secure activation and de-activation of the power transistor is ensured. In this manner, the amplitude in the positive and negative directions remains constant independent of the duty cycle. The galvanically insulated transfer permits the control of a power transistor

whose potential is substantially higher than the potential of the control electronics. The switching speed of the power transistor is determined or delimited by the output resistance of the impulse source on the primary side of the transformer and can thus be optimally adjusted or set. The integrity of the insulation between the control electronic and the power circuit can be ensured to a very high degree by corresponding configuration of the transformer. A further advantage of this switching arrangement is that the size of the components of the transformer are relatively small, which results from the short impulse duration (T1p and T1n) of the impulse to be transferred, as a consequence of which only a reduced winding count is needed to produce the impulse.

Patent Claims

1. A switching arrangement for controlling load-controlled power switches via a transformer which generates positive and negative voltage impulses, wherein

-in the input of the transformer (Ü), voltage impulses (T1p, T1n) in positive and negative directions and having short durations are inputted, these inputted voltage impulses being transformed, by two field effect transistors (F1, F2) connected to the discharge circuits (Ü1,Ü2) at the secondary side of the transformer, into voltage impulses (T3p, T3n) in positive and negative directions for controlling the power switch (LT), the impulse duration of the voltage impulses (T3p, T3n) being extended to the beginning of the next input impulses with reversed voltage directions (T1n, T1p),

-the source terminal of the first field effect transistor (F1) is connected with a discharge circuit (Ü1) and the source terminal of the second field effect transistor (F2) is connected with a different discharge circuit (Ü2),

-the drain terminal of the first field effect transistor (F1) is connected with the gate terminal (G) of the power switch (LT) and the drain terminal of the second field effect transistor (F2) is

connected with a further terminal of the power switch (LT) and whereby

-the gate terminal of the first field effect transistor (F1) is connected via a first resistor (R1) with the drain terminal of the second field effect transistor (F2) and the gate terminal of the second field effect transistor (F2) is connected via a second resistor (R2) with the drain terminal of the first field effect transistor (F1).

2. A switching arrangement according to 1 characterized in that a respective zener diode is connected in series with each of the first and second resistors (R1, R2).

3. A switching arrangement for controlling load-controlled power switches via a transformer which generates positive and negative voltage impulses, wherein

-in the input of the transformer (Ü), voltage impulses (T1p, T1n) in positive and negative directions and having short durations are inputted, these inputted voltage impulses being transformed, by two field effect transistors (F1, F2) connected to the discharge circuits (Ü1,Ü2) at the secondary side of the transformer, into voltage impulses (T3p, T3n) in positive and negative directions for controlling the power switch (LT), the impulse duration of the voltage impulses (T3p, T3n) being

extended to the beginning of the next input impulses with reversed voltage directions (T1n, T1p),

-the source terminal of the first field effect transistor (F1) is connected with a discharge circuit (Ü1) and the source terminal of the second field effect transistor (F2) is connected with a different discharge circuit (Ü2),

-the drain terminal of the first field effect transistor (F1) is connected with the gate terminal (G) of the power switch (LT) and the drain terminal of the second field effect transistor (F2) is connected with a further terminal of the power switch (LT) and whereby

-the gate terminal of the first field effect transistor (F1) is connected via a series switch having a first resistor (R1) and a first zener diode (Z1) with the source terminal of the second field effect transistor (F2) and the gate terminal of the second field effect transistor (F2) is connected via a series switch having a second resistor (R2) and a second zener diode (Z2) with the source terminal of the first field effect transistor (F1).

4. A switching arrangement for controlling load-controlled power switches via a transformer which generates positive and negative voltage impulses, wherein

-in the input of the transformer (Ü), voltage impulses (T1p, T1n) in positive and negative directions and having short durations are inputted, these inputted voltage impulses being transformed, by two field effect transistors (F1, F2) connected to the discharge circuits (Ü1,Ü2) at the secondary side of the transformer, into voltage impulses (T3p, T3n) in positive and negative directions for controlling the power switch (LT), the impulse duration of the voltage impulses (T3p, T3n) being extended to the beginning of the next input impulses with reversed voltage directions (T1n, T1p),

-the source terminal of the first field effect transistor (F1) is connected with a discharge circuit (Ü1) and the source terminal of the second field effect transistor (F2) is connected with a different discharge circuit (Ü2),

-the drain terminal of the first field effect transistor (F1) is connected with the gate terminal (G) of the power switch (LT) and the drain terminal of the second field effect transistor (F2) is connected with a further terminal of the power switch (LT) and whereby

-the gate terminal of the first field effect transistor (F1) is connected via a series switch having a first resistor (R1) and a first zener diode (Z1) with the source terminal of the second field

effect transistor (F2) and the gate terminal of the second field effect transistor (F2) is connected via a second resistor (R2) with the drain terminal of the first field effect transistor (F1).

5. A switching arrangement according to 4, characterized in that a second zener diode (Z2) is connected in series with the second resistor (R2).

6. A switching arrangement for controlling load-controlled power switches via a transformer which generates positive and negative voltage impulses, wherein

-in the input of the transformer (Ü), voltage impulses (T1p, T1n) in positive and negative directions and having short durations are inputted, these inputted voltage impulses being transformed, by two field effect transistors (F1, F2) connected to the discharge circuits (Ü1,Ü2) at the secondary side of the transformer, into voltage impulses (T3p, T3n) in positive and negative directions for controlling the power switch (LT), the impulse duration of the voltage impulses (T3p, T3n) being extended to the beginning of the next input impulses with reversed voltage directions (T1n, T1p),

-the source terminal of the first field effect transistor (F1) is connected with a discharge circuit (Ü1) and the source terminal

of the second field effect transistor (F2) is connected with a different discharge circuit (Ü2),

-the drain terminal of the first field effect transistor (F1) is connected with the gate terminal (G) of the power switch (LT) and the drain terminal of the second field effect transistor (F2) is connected with a further terminal of the power switch (LT) and whereby

-the gate terminal of the first field effect transistor (F1) is connected via a first resistor (R1) with the drain terminal of the second field effect transistor (F2) and the gate terminal of the second field effect transistor (F2) is connected via a series switch having a second resistor (R2) and a second zener diode (Z2) with the source terminal of the first field effect transistor (F1).

7. A switching arrangement according to 6, characterized in that a first zener diode (Z1) is connected in series with the first resistor (R1).

8. A switching arrangement according to one or more of claims 1 to 7, characterized in that a third resistor (R3) is connected between the gate terminal (G) and a further terminal of the power switch (LT).

9. A switching arrangement according to one or more of claims 1 to 7, characterized in that a MOS-FET (metal oxide semiconductor field effect transistor) or an IGBT (insulated gate bipolar transistor) is used as the power switch (LT).

10. A switching arrangement according to one or more of claims 1 to 7, characterized in that the duration of the voltage impulse (T1p, T1n) inputted into the input of the transformer (Ü) does not exceed five µs and is less than or equal to the duration of the activation impulse (T3p) and less than or equal to the de-activation impulse (T3n) of the power switch (LT).

11. A switching arrangement according to one or more of claims 1 to 7, characterized in that a respective diode (D1, D2) is disposed between each of the field effect transistors (F1, F2) between the source terminal (S) and the drain terminal (D) thereof.

12. A switching arrangement according to one or more of claims 1 to 9, characterized in that an input capacitance (C) is disposed in the power switch (LT) between the gate terminal (G) and a further terminal (S).

13. A switching arrangement according to claims 1 to 12, characterized in that the two field effect transistors (F1, F2) effect a transformation of the two input impulses (T1p, T1n) into

respective longer impulses of which one effects the activation of power switch (LT) and the maintenance of the power switch (LT) in its activated condition and the other effects the de-activation of the power switch (LT) and maintenance of the power switch (LT) in its de-activated condition.

14. A switching arrangement according to 13, characterized in that the duration of the period (T) of the impulse (T1p, T1n) inputted into the input of the transformer (Ü) corresponds to the durations of the periods (T3p + T3n) of the impulses (Tp3, T3n) necessary for the control of the power switch (LT).

15. A switching arrangement according to one or more of claims 1 to 7, characterized in that the durations of the periods of the impulse (T3p, T3n) at the power switch (LT) can have a predetermined relationship with one another (duty cycle).

16. A switching arrangement according to one or more of claims 1 to 7, characterized in that the use of a transformer (Ü) with oppositely sensed windings of the primary and secondary sides thereof determines the voltage direction of the impulse at the power switch (LT).

Abstract Of The Disclosure

In a switching arrangement for controlling a load-controlled power switch via a transformer Ü, a voltage signal is inputted into the transformer, the voltage signal being comprised of impulses of short duration T1p, T1n in positive and negative directions. Two field effect transistors F1, F2 at the secondary side of the transformer Ü convert the impulses T1p, T1n into impulses T3p, T3n in positive and negative directions which reliably control the power switch LT, the impulse duration of the impulses T3p, T3n being extended to the beginning of the next input impulses with reversed voltage directions T1n, T1p. A diode D1 and D2, respectively, is disposed in each of the field effect transistors F1 and F2 between the source terminal S and the drain terminal D thereof. A respective series switch is activated ahead of the gate terminals of each respective field effect transistor F1 and F2.

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Fig. 1

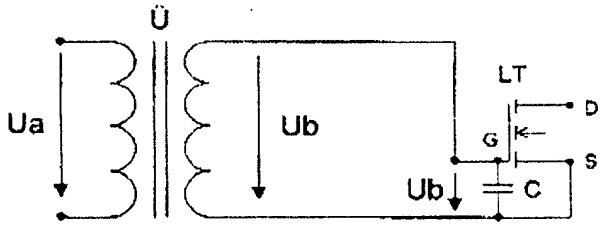

Fig. 1 corrsponds to the prior art

Fig 2

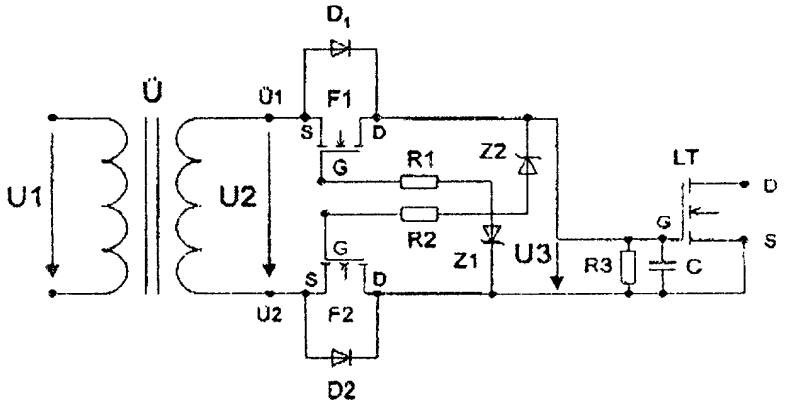

Fig. 3

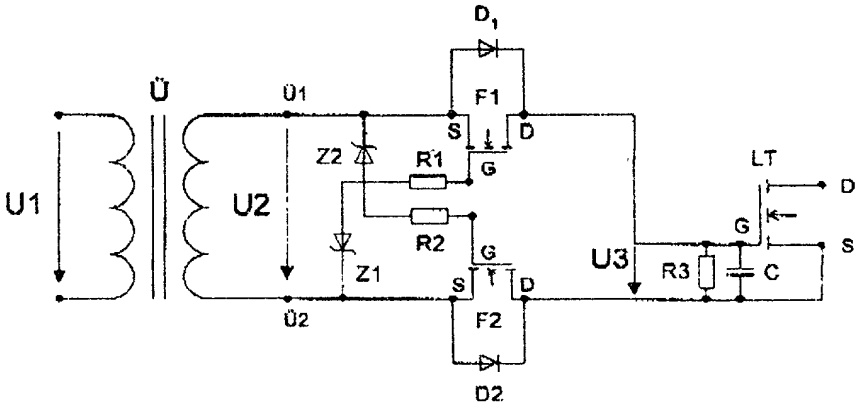

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Fig. 4

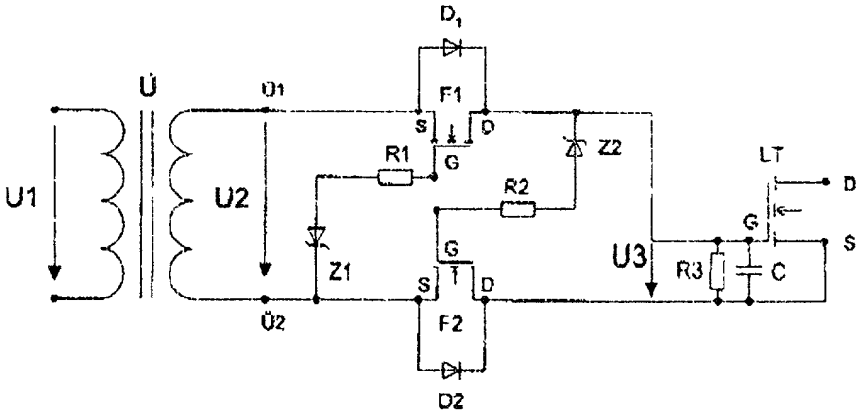


Fig. 5

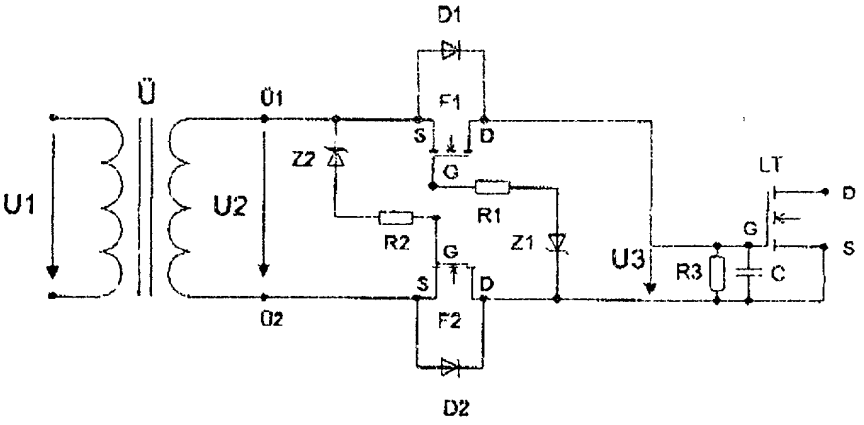
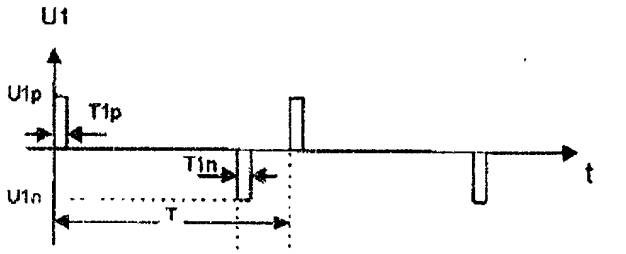


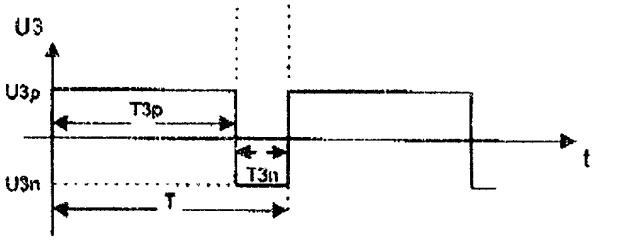
Fig. 6



U1p = (-U1n) U3p = (-U3n)

T1p = T1n

Fig. 7



COMBINED DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, we hereby declare that:

Our residences, post office addresses and citizenships are as stated below next to our names; we believe *are the original*, first and joint inventors of the subject matter which is claimed and for which a patent is sought of the invention entitled:

A SWITCHING ARRANGEMENT FOR GALVANICALLY INSULATED CONTROL OF A LOAD-CONTROLLED POWER SWITCH

the specification of which

_____ is attached hereto;
xx was filed on 07 February 2000 as International Application Ser. No. PCT/EP00/00368 and is amended herewith.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose all information known to me to be material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Applications:			Priority Claimed:	
199 05 500.9	Germany	10 February 1999	X	
199 63 330.4	Germany	27 December 1999	X	
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below:

_____
(Application Number) (Filing Date)

I hereby appoint attorney Robert W. Becker, Reg. No. 26,255, to prosecute this application and to transact all business in the Patent and Trademark Office connection therewith. Address all telephone calls to (505) 286-3511. Address all correspondence to ROBERT W. BECKER & ASSOCIATES, 11896 N. Highway 14, Suite B, Tijeras, New Mexico 87059.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Post Office Address: Same as Above

United States Patent & Trademark Office

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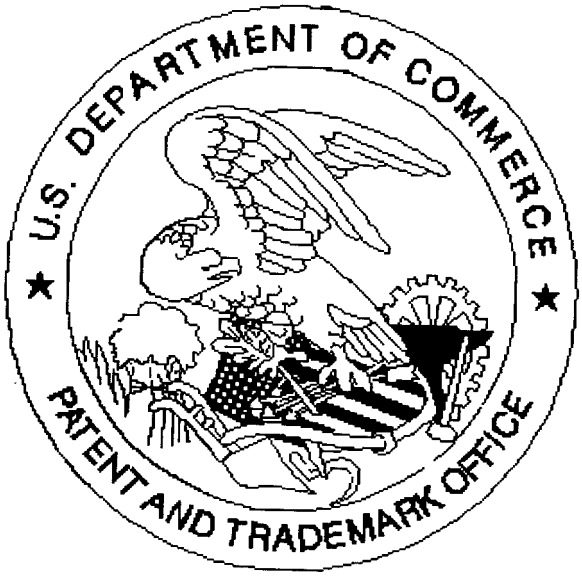

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